INTERFACE

MAINTENANCE MANUAL

FOR

GERBER SERIES 1200

GRAPHIC DISPLAY

SYSTEM

INSTRUCTION MANUAL

THE GERBER SCIENTIFIC INSTRUMENT COMPANY

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Contractor: THE GERBER SCIENTIFIC INSTRUMENT COMPANY

Contractors Order No: 20998 Contractors Work Order No: 73-441

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INTERFACE MAINTENANCE MANUAL FOR GERBER SERIES 1200 GRAPHIC DISPLAY SYSTEM

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THE GERBER SCIENTIFIC INSTRUMENT COMPANY
HARTFORD, CONNECTICUT 06101

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C-24012	Sheet 2 of 2
C-23902	Sheet 1 of 2
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1.0 GENERAL DESCRIPTION

The Gerber Series 1200 Interface System is composed primarily of two printed circuit cards; the GHP-1 and GDP-1. The GHP-1 card provides the required interface circuitry for the mating of the Gerber Series 1200 System with the Hewlett Packard HP2114A computer. The GDP-1 card provides the necessary circuitry for interfacing the High-Speed Paper Tape Reader, or the Model M-12 Magnetic Tape Unit, to the HP2114A computer.

1.1 SCOPE

This manual is written for those persons thoroughly familiar with digital logic techniques. A basic understanding of software functions will also prove helpful.

Section 2 and Section 3 of this manual provide descriptive data covering the GDP-1 and GHP-1 cards, respectively. Logic Drawings are provided at the rear of this manual. These drawings are for reference only and will not reflect any system changes occurring after the publication date of this manual.

System documentation covering the computer and other system components should be available for reference when utilizing this manual for troubleshooting purposes.

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2.0 READER INTERFACE CARD (GDP-1)

The GDP-1 Reader/M-12 Interface Printed Circuit Board provides for direct interfacing of a Digitronics 2540 paper tape reader and/or an M-12 Magnetic Tape Unit to the Hewlett Packard HP2114A computer.

2.1 GENERAL

The GDP-1 card is a two-sided board and is keyed on one edge to insure proper connection with the receptacle in slot 10 of the computer I/O section. The larger terminal edge is numbered 1 through 85 on the component side and 2 through 86 on the opposite side. The top edge of the board has terminals numbered 1 through 24 on the component side. The opposite side uses alpha characters. Characters G, I, O and Q are not used.

The circuit card plugs directly into the Input/Output (I/O) section of the computer (slot 10). The inputs from the Reader and M-12 Unit plug directly into a connector on the top edge of the card. Also included in the circuitry is the Reader forward/reverse and rewind control for a Digitronics 6040 tape handler.

Selection of the Paper Tape Reader or the M-12 Magnetic Tape Unit is made by a switch located on the teletypewriter control panel.

2.2 CIRCUIT DESCRIPTION (See Drawing C24012)

Each I/O instruction of the computer

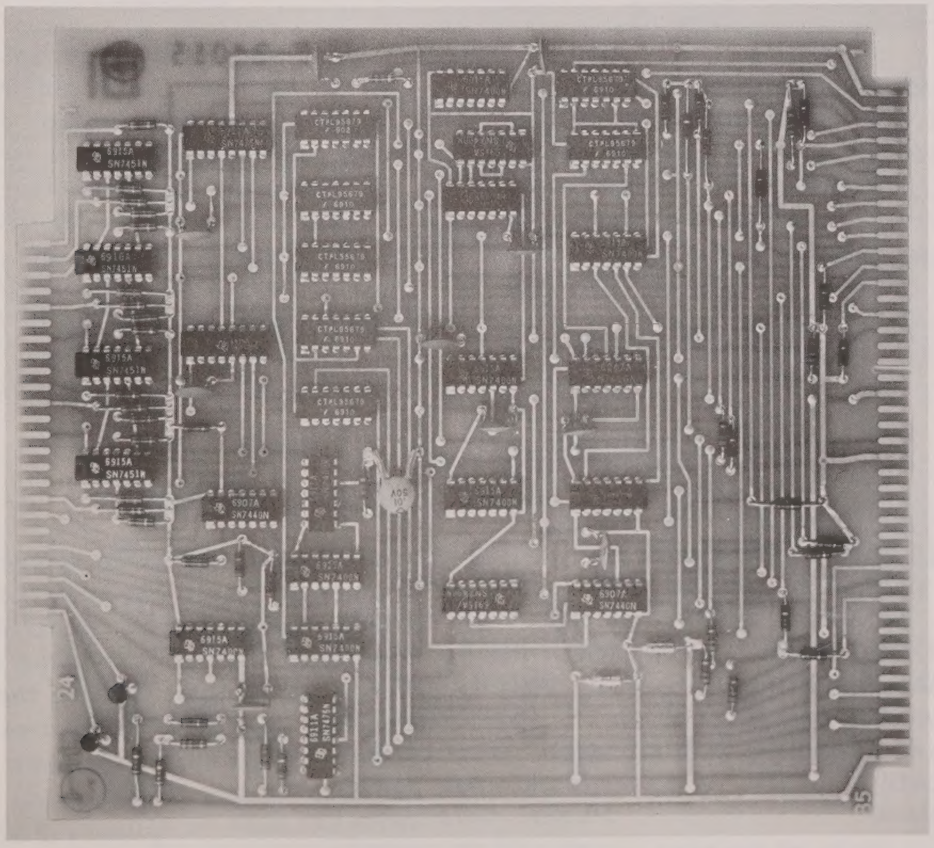

Figure 2-1. GDP-1 READER CARD

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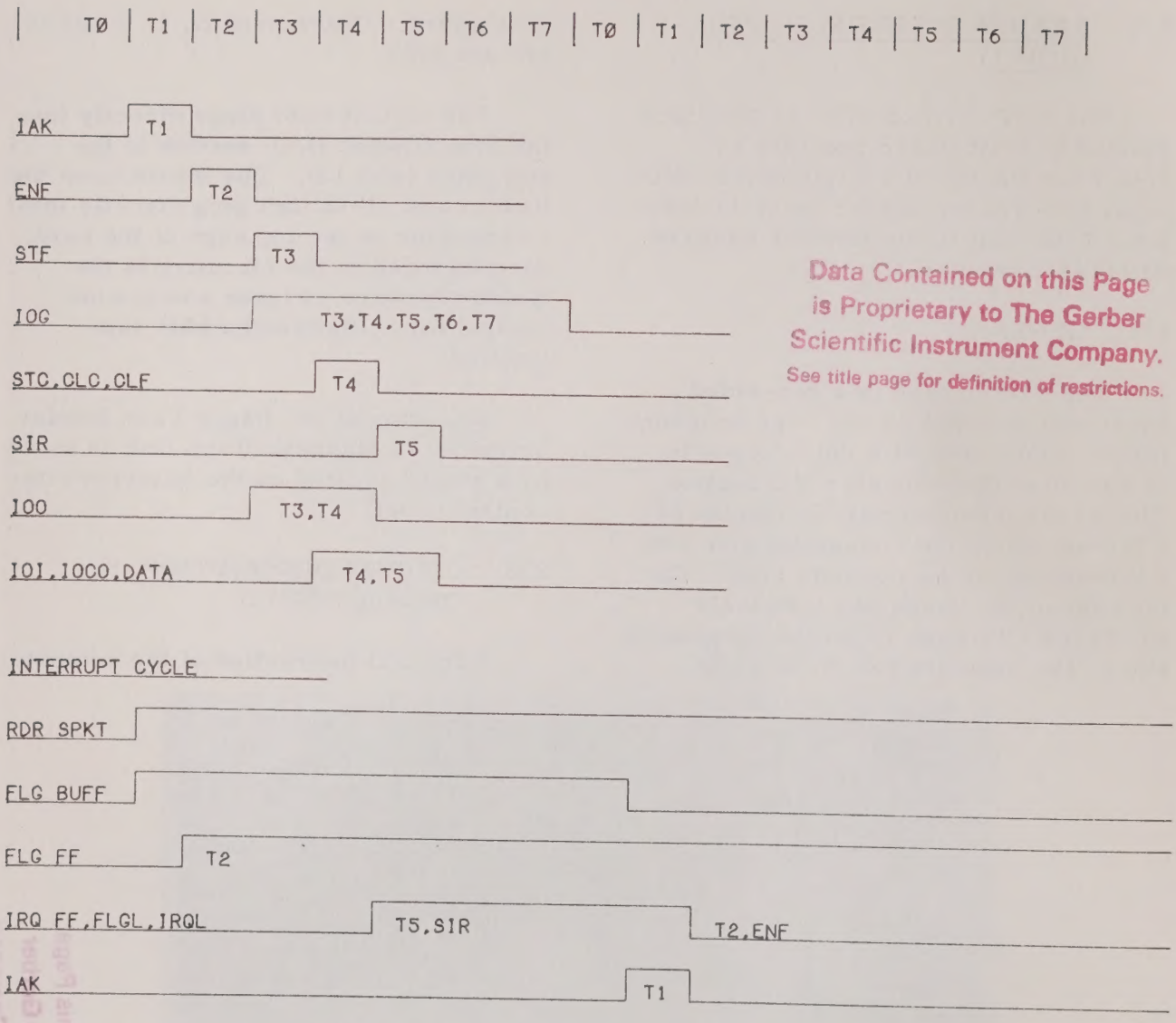

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Figure 2-2. READER TIMING DIAGRAM

is associated with a select code to identify the peripheral device to be controlled. This code appears as the SCM (pin 14), SCL (pin 16), and IOG (pin 15) on the computer connector. All controls from the computer to the interface card are gated with signals IC5B and IC4D.

A typical cycle of the tape reader would begin with the occurrence of signals STC (pin 22) and CLF (pin 7). These signals set the control and drive flip-flops and reset the flag and flag buffer flip-flops. Setting the drive flip-flop energizes the forward pinch roller and releases the tape reader brake, causing the tape to advance. When a sprocket hole is sensed, a positive reader sprocket signal appears on pin X*. The

leading edge of this signal is differentiated (IC11A and IC11B), resetting the drive flip-flop and setting the flag buffer flip-flop. This pulse also strobes data from the reader into a buffer register (IC24 and IC25). The data is now ready to be gated into the I/O bus of the computer.

Data transfer to the computer I/O bus is accomplished by a LIA or LIB instruction. Either of these instructions generates an IOI signal (pin 24) which strobes and gates IC24 through IC27 with data in the buffer, and transfers data to the I/O bus. The computer detects an SFS instruction (pin 25) to determine when the reader has advanced one character. This causes an SKF signal (pin 12) to be output when the flag flip-flop is set.

2.2.1 Interrupt Operation

If the interrupt system has been enabled, IEN (pin 8) will be true. The STC and CLF instructions initiate the reader as described in Paragraph 2.2. When the sprocket signal is sensed, the flag buffer flip-flop is set. At ENF time (pin 46, see Figure 2-2) the flag flip-flop is also set. If a higher priority device is not interrupting, PRH (pin 23) will be true. As a result, the IRQ flip-flop will be set at SIR time (pin 32). The PRL signal (pin 3) will be forced false to prevent an interrupt by a lower priority device, until the current interrupt is complete. During the next machine cycle, the IAK signal (pin 10) resets the flag buffer flip-flop and the IRQ flip-flop.

2.2.2 Reader/M-12 Selection

Pins 18* and V* are inputs from a remote switch which will determine which unit is to be the input device. IC20 through IC23 gate each set of 8 data lines with the selected switch signal. Also gated is the Reader Sprocket or M-12 MOSP signal. On the output gating structure, the Reader Stop, Forward or Reverse and M-12 RRF signals are gated by this switch signal (M-12 SW and RDR SW).

2.2.3 Forward, Reverse and Rewind Control

An OTA or OTB instruction generates an IOO signal (pin 20). The IOO signal, in conjunction with the appropriate output bit on the I/O bus (IOBO 15, IOBO 14 or IOBO 13) sets the reader reverse flip-flop, spooler rewind flip-flop or spooler fast forward flip-flop. When the reader reverse flip-flop is set, control of the drive flip-flop is switched to the reader reverse line (pin Y*).

Table 2-1. GDP-1 MNEMONICS

Mnemonic	Pin No.	Definition	Drawing C-24012 Sheet No.
CLC	21	Clear Control	1
CLF	7	Clear Flag	1
CRS	13	Control Reset	1
ENF	46	Enable Flag	1
FLGL	4	Flag Signal Lower Select Code	1
IAK	10	Interrupt Acknowledge	1
IC		Integrated Circuit	1 and 2
IEN	8	Interrupt Enable	1
IOG	15	Input/Output Group	1

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Table 2-1. (Continued)

GDP-1 MNEMONICS

Mnemonic	Pin No.	Definition	Drawing C-24012 Sheet No.
IOI	24	Input Strobe	2
IOO	20	Output Strobe	1
IOBI	(see Drawing)	Computer Bus In	2
IOBO	(see Drawing)	Computer Bus Out	2
IRQL	6	Interrupt Request	1
LIA		Load "A" Register	Program Instruction
LIB		Load "B" Register	Program Instruction
M-12 RRF	Z*	Run MT Reader	2
M-12 SW	18*	Select M-12	2
M-12 XX	(see Drawing)	Mag Tape Channels	2
M-12 SPKT		Output Sprocket	1
OTA		Output to "A" Register	Program Instruction
OTB		Output to "B" Register	Program Instruction
PRH	23	Priority High	1
PRL	3	Priority Low	1
POPIO	17	Power On Preset	1
RDR FWD	22*	Reader Forward	2
RDR REV	Y*	Reader Reverse	2
RDR STOP	21*	Reader Stop	2
RDR SW	V*	Select Paper Tape Reader	2
RDR XX	(see Drawing)	Paper Tape Channels	2
SCL	16	Select Code, LSB	1
SCM	14	Select Code, MSB	1
SFC	5	Skip if Flag Clear	1
SFS	25	Skip if Flag Set	1
SKF	12	Skip Flag	1
SIR	32	Set Interrupt Request	1
SPKT	20*, X*	Reader Sprocket	1
SRQ	19	Service Request	1
STC	22	Set Control	1
STF	9	Set Flag	1
Spooler, Fast Forward	24	Spooler, Fast Forward	2
Spooler Rewind	23	Spooler, Rewind	2

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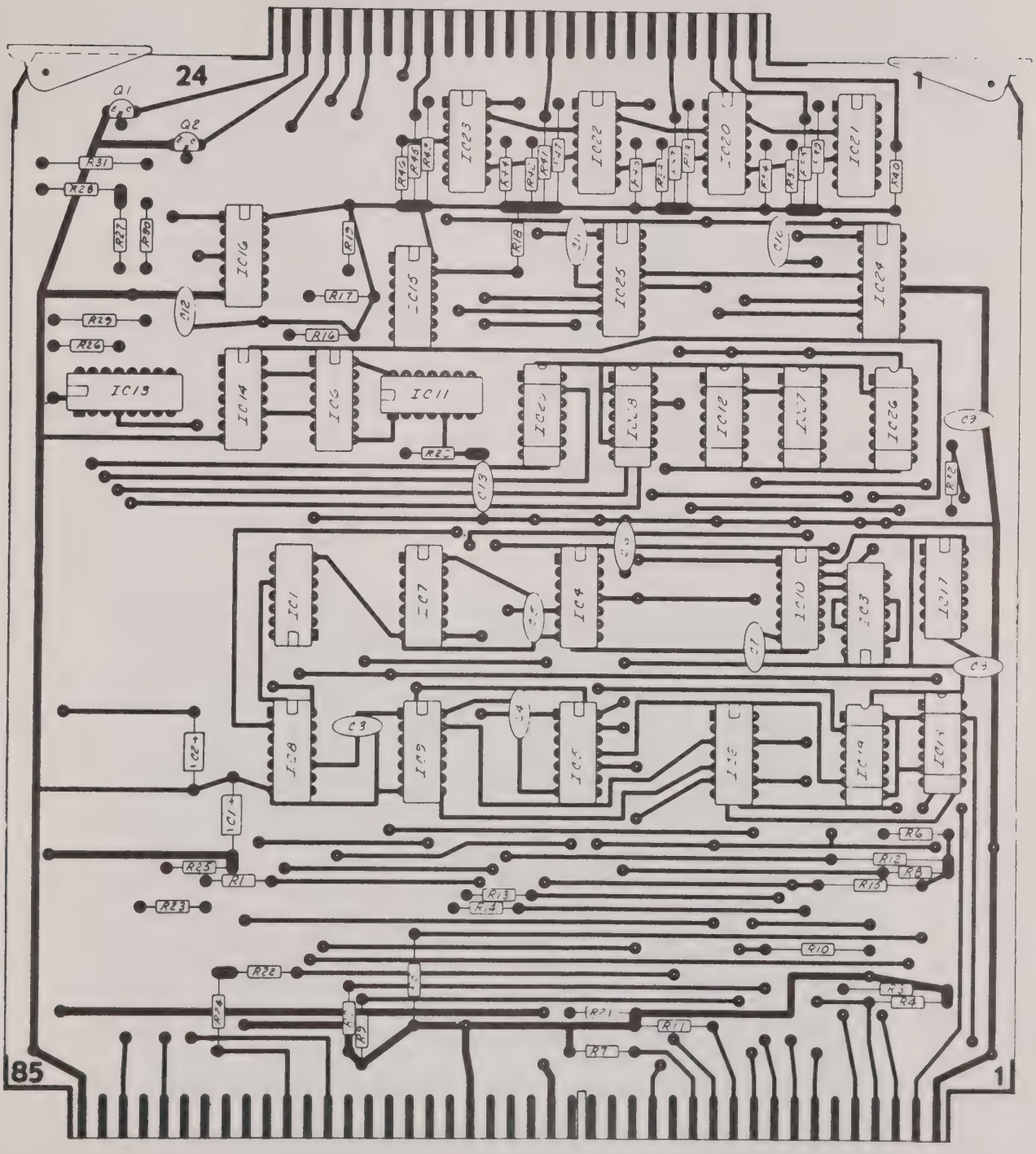

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Figure 2-3. GDP-1 LAYOUT

Table 2-2. GDP-1 PARTS LIST

Quantity	Part No.	Print Ref.	Description
1	D24014		Printed Circuit Board - Detail
1	D24013		Printed Circuit Board - Artwork
2	952-031006	Q1, Q2	Transistor
10	298-020104	IC1 thru IC4, IC6, IC7, IC11, IC14, IC16, IC17	Integrated Circuit
3	298-020106	IC5, IC9, IC10	Integrated Circuit
2	298-020105	IC8, IC15	Integrated Circuit
4	298-020103	IC20, IC21 thru IC23	Integrated Circuit
3	298-020102	IC13, IC24, IC25	Integrated Circuit
7	298-030102	IC12, IC18, IC19, IC26 thru IC29	Integrated Circuit
2	765-007294	R20, R32	Resistor, 180 ohm, 1/4W, 5%
22	765-007394	R16 thru R19, R26, R29, R33 thru R48	Resistor, 1K, 1/4W, 5%
22	765-007414	R1 thru R15, R21 thru R25, R27, R30	Resistor, 1.5K, 1/4W, 5%
2	765-007515	R28, R31	Resistor, 8.2K, 1/4W, 5%
11	264-426010	C3 thru C13	Capacitor, .01 μf, 50V
2	264-801444	C1, C2	Capacitor, 1 μf, 35V DC
2	688-117002		Pin, Groove
2	528-140201		Extractor

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3.0 SYSTEM INTERFACE CARD (GHP-1)

The GHP-1 System Interface Printed Circuit Board provides for direct interfacing of Gerber Drafting Table Systems to the Hewlett-Packard HP-2114A computer (See Drawing C-23902).

3.1 GENERAL

The GHP-1 card is a two-sided board and is keyed on one edge to insure proper connection with the receptacle in slot 17 of the computer I/O section. The larger terminal edge (LP) is numbered 1 through 85 on the component side, and 2 through 86 on the opposite side. The top edge of the board has a 70 pin connector using both alpha and numeric characters.

The circuit card plugs directly into the Input/Output (I/O) section of the computer (slot 17). The inputs from the SMD motor driver cabinet plug directly into a connector on the top edge of the card, through the connector panel.

The GHP-1 card is made up of dual-in-line integrated circuit (IC) sockets, and is specifically wire wrapped for a given circuit configuration, based on customer requirements. The card has twelve, 16 pin I/C sockets and sixty, 14 pin I/C sockets.

3.2 MOTOR PULSE GENERATION

All signals from the computer are gated with the select code (LSCL, LSCM, and IOG) for the particular I/O slot in

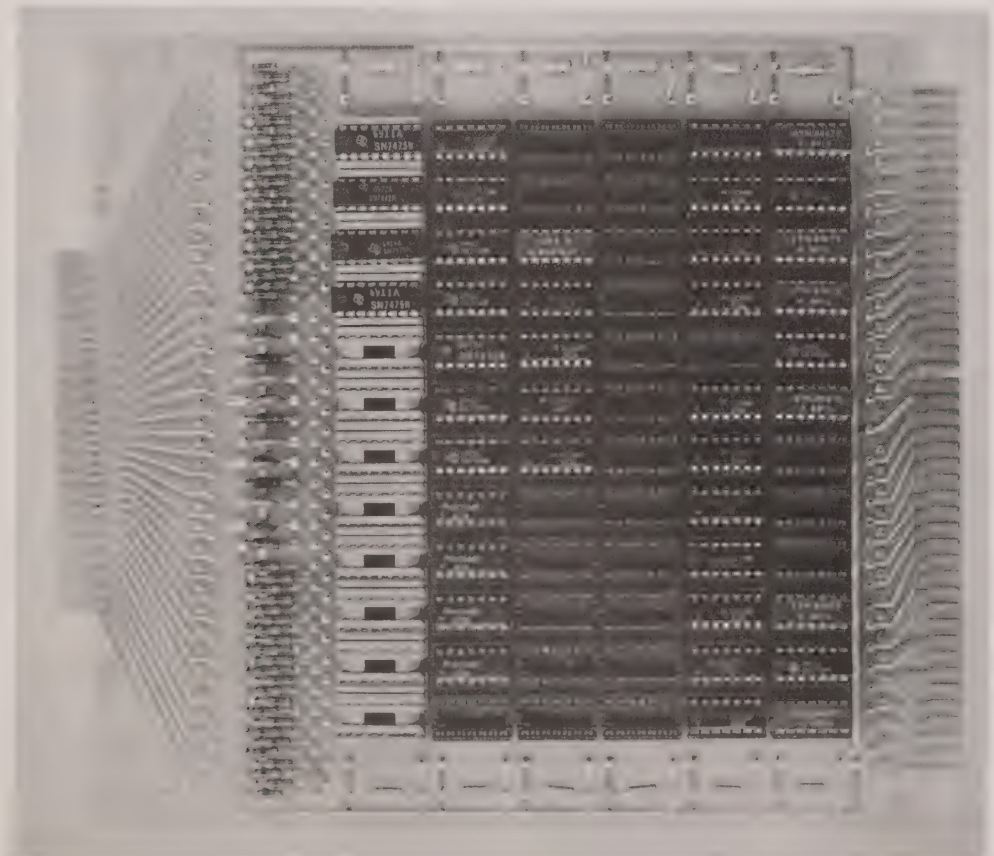

Figure 3-1. GHP-1 INTERFACE CARD

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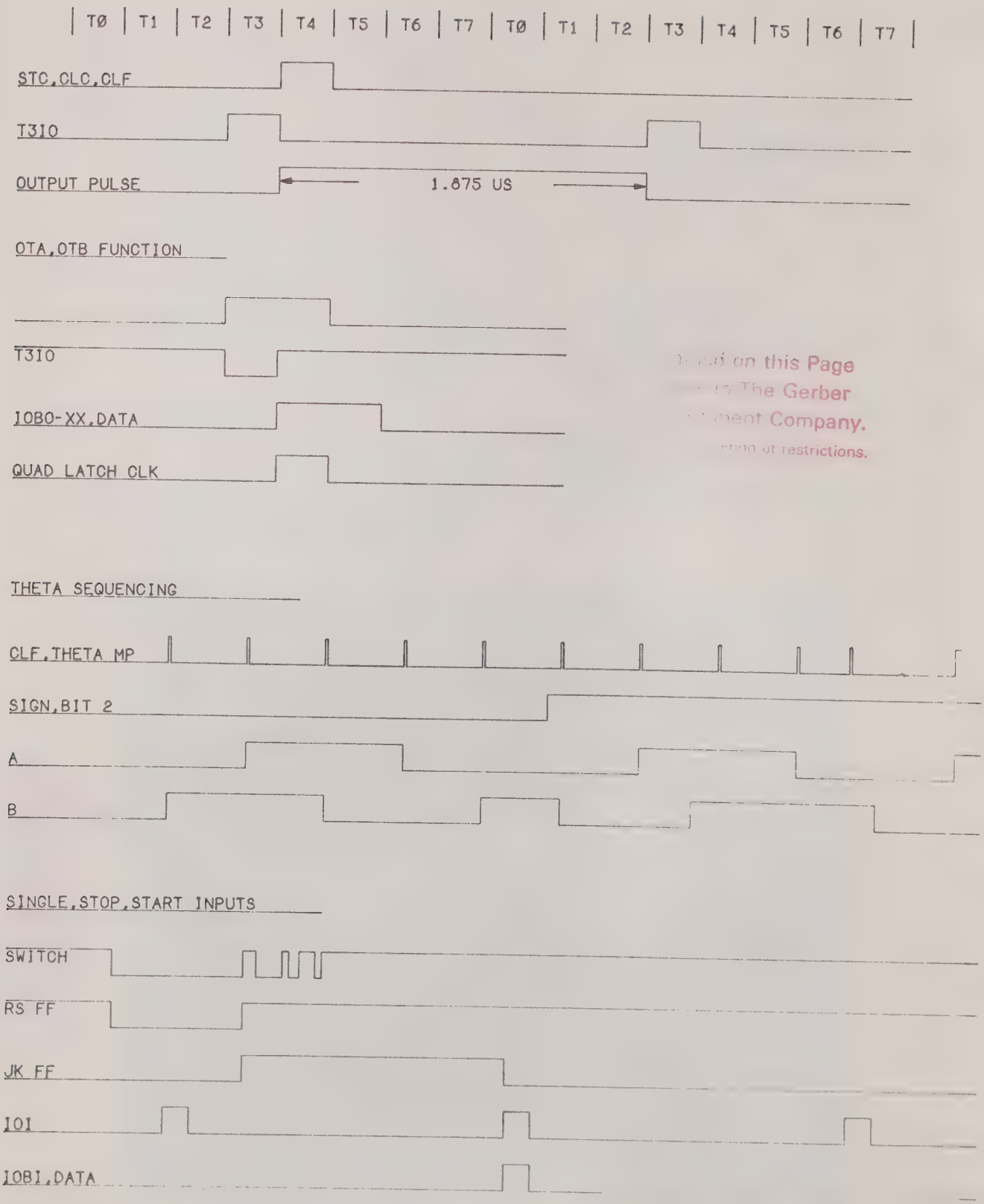

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Figure 3-2. INTERFACE TIMING DIAGRAM

the computer. It should be noted that the I/O slots are assigned addresses 10 through 17. The STC, CLC, CLF instructions are used to generate motor pulses. The major and minor axis motor pulses must travel over long lengths of cable. The STC, CLC signals are 125 ns long, and therefore must be lengthened for proper system operation. A flip-flop is set by STC or CLC and reset by T3IO, therefore lengthening the pulses to approximately 1.8 μs. Bit 3 determines which axis (A or B) is major and routes the MJP and MNP signals accordingly. If the system is equipped with a VAPE head (optional) these motor pulses may be routed to control the VAPE head blade motors (U and V axis) if the bit 8 flip-flop is set. Also, gate 23 generates MP for the OEH-B option, if the VAPE flip-flop is not set and the shutter is open. This action will inhibit any filter motion except for legitimate line drawing.

The X, Y, U and V sign are taken directly from bit 0 and bit 1 flip-flops.

3.3 OUTPUT BITS

The OTA and OTB instructions generate the IOO signal. This signal is anded with T3IO and the select code, and clocks data from the I/O bus into the latch type flip-flops.

Bits 4, 5, 6 and 7 are decoded using a BCD to decimal decoder to generate pen and shutter signals. Bit 7 enables the decoder and may be inhibited or overridden by the pen switch.

The decoded 7 is either the OEH-B shutter signal or VAPE shutter signal, depending upon the state of the bit 8 flip-flop. The OEH-B shutter signal will also operate pen 1 if the PHOTO-PEN switch on the OEH-B is in the PEN position. This arrangement allows pen plots to be drawn with shutter commands.

The bit 9 flip-flop activates the Absolute Reference Point (Precision Limit) switches either on the drafting table or on the VAPE head, depending on the state of bit 8.

3.4 THETA SEQUENCING (CUTTER)

The CLF signal generates clock pulses for the Theta Sequencer with the bit 2 flip-flop determining the sign. Outputs from the A and B flip-flops are taken for the MA1, MA2, MA3 and MA4 signals. These MA signals are amplified by a GLP-2 solenoid driver card to run the cutter rotation stepmotor.

3.5 INPUT BITS

Signals from the Slew switches, Limit switches, Precision Limit Zero, Cutter Home and VAPE Lamp OK are strobed onto the I/O bus by the IOI signal which has been gated with the select code.

The Single, Stop and Start switches are buffered before being strobed onto the I/O bus.

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Table 3-1. GHP-1 MNEMONICS (See title page for definition of [illegible])

Mnemonic	Pin No.	Definition	Drawing C-23902 Sheet No.
θ Sign		Cutter Rotation Sign	1
APE		VAPE Control Bit	2
ALLS2	A29	Table A Left Limit Switch	2
APEZP		VAPE RTPL	1

Table 3-1. (Continued)

GHP-1 MNEMONICS

Mnemonic	Pin No.	Definition	Drawing C-23902 Sheet No.
APSA	B8	VAPE A Sign	1
APSB	B10	VAPE B Sign	1
ARLS2	A28	Table A Right Limit Switch	2
ASIGN	A2	A Stepmotor Sign	1
ASTMP	A1	A Stepmotor Pulse	1
BLLS2	A31	Table B Left Limit Switch	2
BRLS2	A30	Table B Right Limit Switch	2
BSIGN	A4	B Stepmotor Sign	1
BSTMP	A3	B Stepmotor Pulse	1
CLC	21	Clear Control	1
CLF	7	Clear Flag	1
CTH		Cutter Home	2
FLASH	B11	VAPE Shutter Open	1
IOBI	(See Drawing)	I/O Bit In	2
IOBO	(See Drawing)	I/O Bit Out	1
IOG	15	I/O Group	1
IOI	24	I/O Input Pulse	1
IOO	20	I/O Output Pulse	1
LPOK		VAPE Lamp OK	2
LSCL	16	Select Code, Least Significant Digit	1
LSCM	14	Select Code, Most Significant Digit	1
MA	A12 thru A15	Phased Cutter Motor Signals	1
MJA		Major Axis	1
MJP		Major Pulse	1
MNP		Minor Pulse	1
POPIO	17	Power On Preset	1
PND	A5 thru A10	Pen Down	1
RTPL		Run to Precision Limit Switches	1
SHUTTER	A11	Shutter Open	1
SINGLE		Single Cycle Switch	2
STC	22	Set Control	1
START		Start Cycle Switch	2
STOP		Stop Cycle Switch	2
SZ	B1	Table Precision Limit Zero	2
T3IO	11	T3 Timing Signal	1
ULSM	B15	VAPE U Minus Limit Switch	2
ULSP	B14	VAPE U Plus Limit Switch	2
USTMP	B7	U Stepmotor Pulse	1
VLSM	B17	VAPE V Minus Limit Switch	2
VLSP	B16	VAPE V Plus Limit Switch	2
VSTMP	B9	V Stepmotor Pulse	1
XDP	B3	X Display Pulse	1

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Table 3-1. (Continued)

GHP-1 MNEMONICS

Mnemonics	Pin No.	Definition	Drawing C-23902 Sheet No.
XSD	B4	X Sign to Display	1
XSIGN		X Sign Flip-Flop	1
+XSLEW	A22	X+Slew Switch	2
-XSLEW	A23	X-Slew Switch	2
YDP	B5	Y Display Pulse	1
YSD	B6	Y Sign to Display	1
YSIGN		Y Sign Flip-Flop	1
+YSLEW	A24	Y+Slew Switch	2
-YSLEW	A25	Y-Slew Switch	2
ZRES	B18	VAPE Precision Limit Zero	2
ZSPB	B2	Table RTPL	1

Table 3-2. SUMMARY OF I/O FUNCTIONS

IOBO (Output)	BIT	IOBI (Input)
ASIGN	Ø	SLEW X+
BSIGN	1	SLEW X-
THETA SIGN	2	SLEW Y+
MAJOR AXIS (B=1)	3	SLEW Y-
PEN BITS (See Table 3-3)	4	ARLS or ULSP
	5	ALLS or ULSM
	6	BRLS or VLSP
PEN ENABLE	7	BLLS or VLSM
VAPE HEAD	8	PREC. LIMITS ZERO
RUN TO PREC. LIMITS	9	Not Used
Not Used	10	Not Used
Not Used	11	Not Used
Not Used	12	Cutter Home or VAPE Lamp Fail
Not Used	13	Single Cycle Switch
Not Used	14	Stop Switch
Not Used	15	Start Switch

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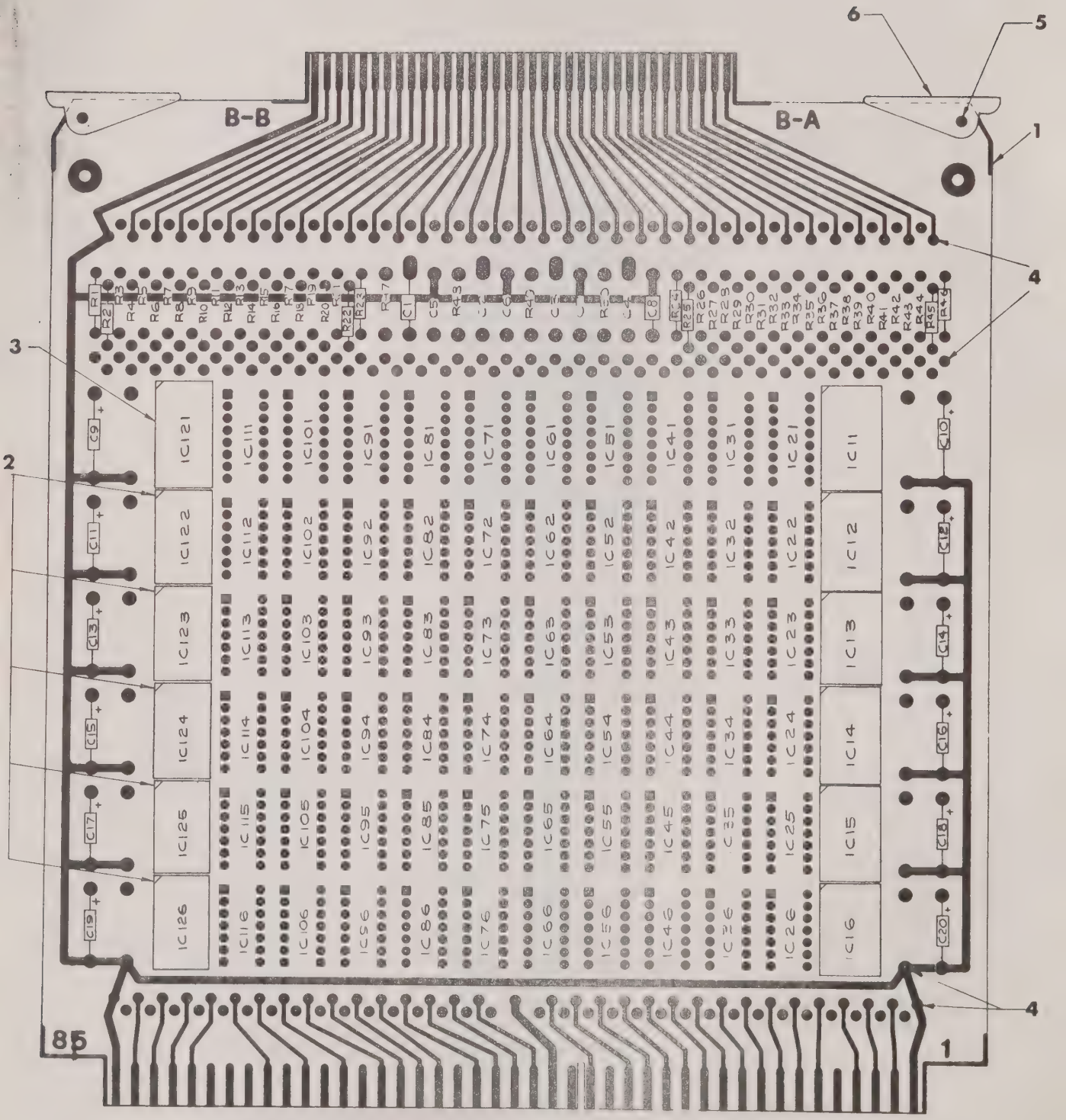

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Figure 3-3. GHP-1 LAYOUT

Table 3-3. PEN BIT FUNCTIONS

Bit 4	Bit 5	Bit 6	Function	
0	0	0	None	
1	0	0	Pen #1	
0	1	0	Six Pen In-Line Only	Pen #2 or Cutter Down
1	1	0		Pen #3
0	0	1		Pen #4
1	0	1		Pen #5
0	1	1		Pen #6
1	1	1	Shutter (OEH or VAPE)	

Table 3-4. GHP-1 PARTS LIST

Quantity	Item No.	Part No.	Print Ref.	Description
1	1	D-23688		Printed Circuit Board-Details
1		D-23687		Printed Circuit Board-Artwork
46		765-007394	R1 thru R47	Resistor, 1K, 1/4W, 5%
4		765-007266	R47 thru R50	Resistor, 100Ω, 1/4W, 5%
4		264-056006	C1 thru C4	Capacitor, 33pf, 100V DC
4		264-056007	C5 thru C8	Capacitor, .0015mf, 100V DC
12		264-801402	C9 thru C20	Capacitor, .1mf, 35V
60	2	880-140203		IC Socket, 14 Pin
12	3	880-140202		IC Socket, 16 Pin
233	4	346-223007		Post, Wire Wrap
2	5	688-117002		Pin, Groove
2	6	528-140201		Extractor
*	*	*		Integrated Circuit

*See Parts List and Drawings furnished with specific system (reference SLB-23704)

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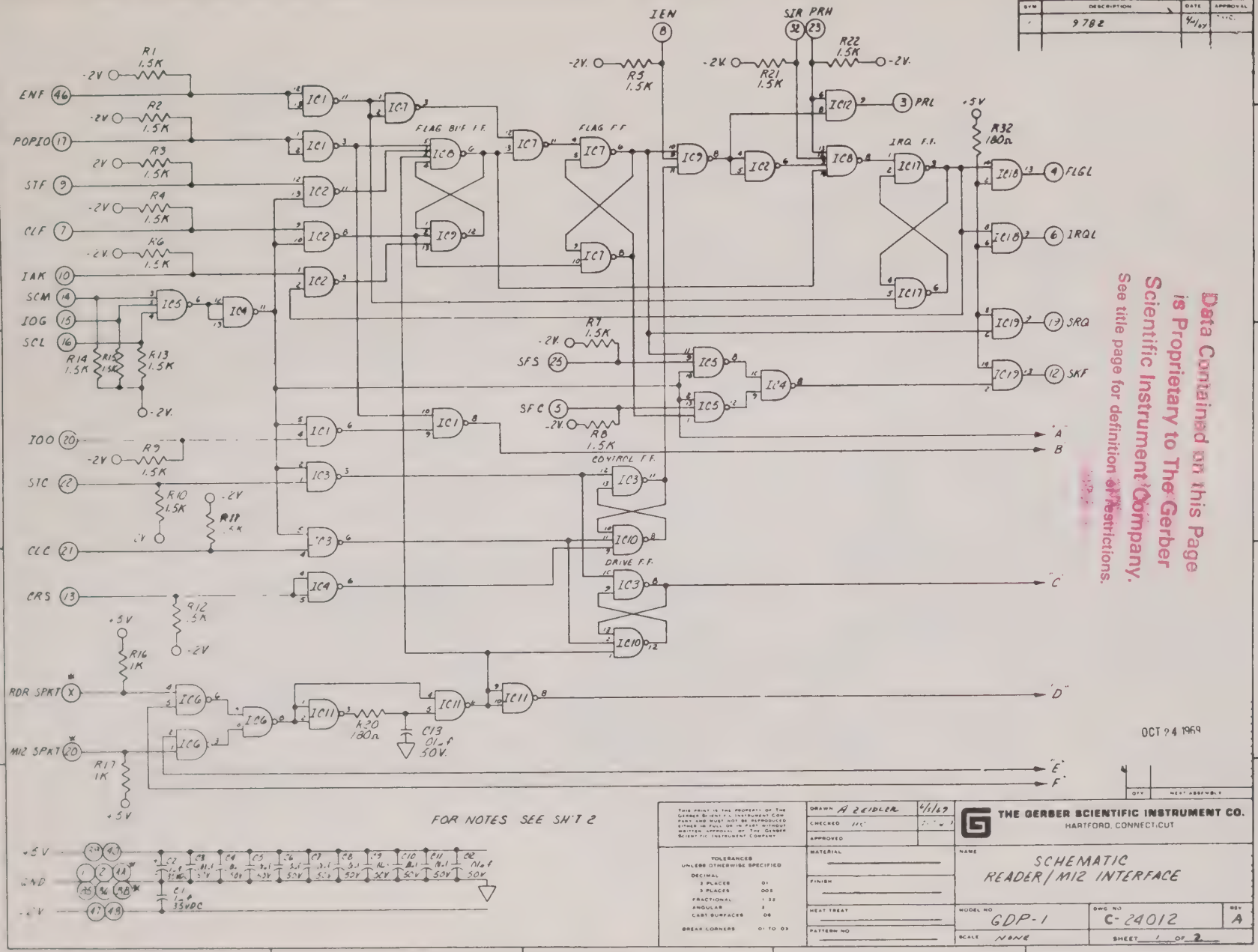

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CHECKED		HARTFORD, CONNECTICUT
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MATERIAL		NAME SCHEMATIC READER/MI2 INTERFACE
FINISH		
HEAT TREAT		MODEL NO GDP-1
PATTERN NO		DWG NO C-24012 REV A
		SCALE NONE SHEET 1 OF 2

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL
2 PLACES .01
3 PLACES .005
FRACTIONAL ± 1/32
ANGULAR ±
CAST SURFACES .06
BREAK CORNERS .01 TO .03

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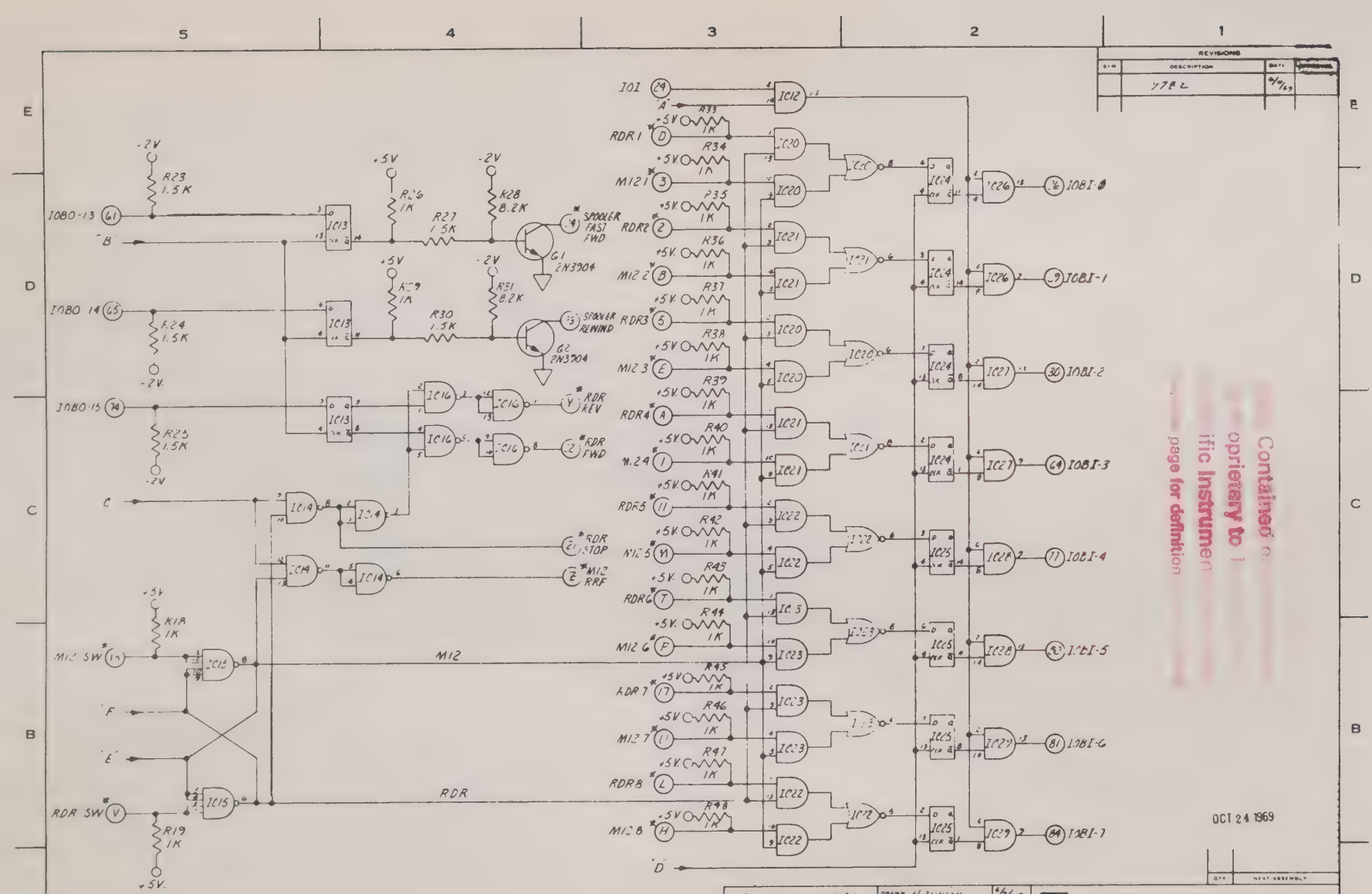

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page for definition

OCT 24 1969

NOTES:
1- FOR ASSEMBLY SEE DWG. D-24015.
2- ALL RESISTORS ARE ¼W 5% UNLESS OTHERWISE SPECIFIED
3- IC1, IC2, IC3 IC4, IC6, IC7, IC11, IC14, IC16 & IC17 ARE SN7430N; IC5 IC9 & IC10 ARE SN7410N; IC20, IC21, IC22 & IC23 ARE SN7453N; IC13, IC24 & IC25 ARE SN7475N; IC12, IC15, IC19, IC26, IC27, IC28 & IC29 ARE CI-19956, IC8 & IC18 ARE SN7404N.
4- IC1 THRU IC11, IC14 THRU IC17, IC20 THRU IC23 HAVE +5V. ON PIN 14 & GND ON PIN 7; IC12, IC13, IC18, IC19, IC24 THRU IC29 HAVE +5V. ON PIN 5 & GND ON PIN 12.
5- * DENOTES PINS ON 48 PIN CONNECTOR.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
	Y7P2	8/9/69	

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DRAWN H. ZEHNER 6/5/69
CHECKED 7-1-69
APPROVED

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL
2 PLACES .01
3 PLACES .005
FRACTIONAL 1/32
ANGULAR 1°
CAST SURFACES .06
BREAK CORNERS .01 TO .03

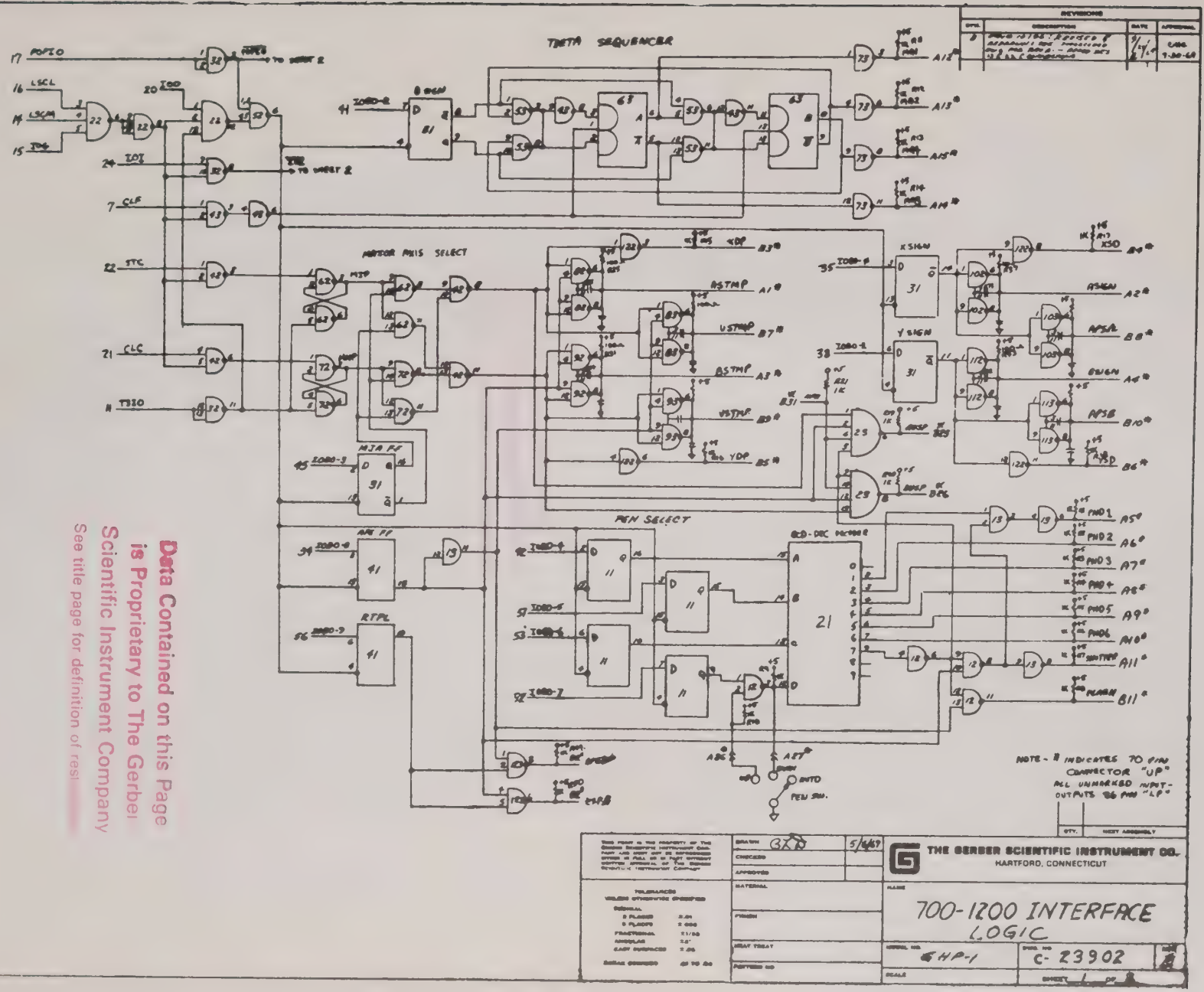
MATERIAL
FINISH
HEAT TREAT
PATTERN NO

THE GERBER SCIENTIFIC INSTRUMENT CO.
HARTFORD CONNECTICUT

NAME
SCHEMATIC
READER/M12 INTERFACE

MODEL NO GDP-1
DWG NO C-24012
REV A
SCALE NONE
SHEET 2 OF 2

QTY NEXT ASSEMBLY



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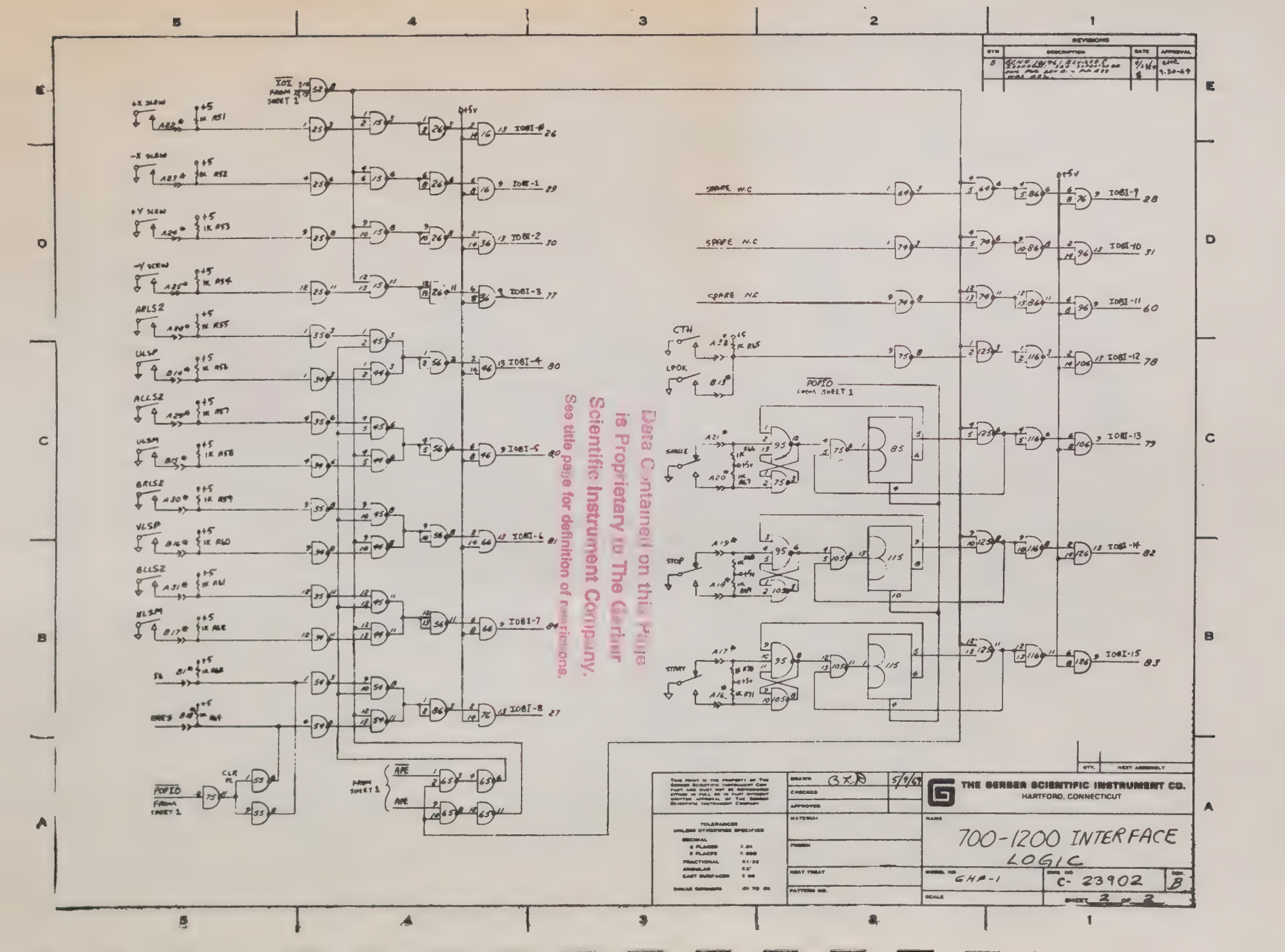
See title page for definition of rest



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REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
B	[illegible]	9/14/67	DATE 9-30-69

THE GERBER SCIENTIFIC INSTRUMENT CO.
HARTFORD, CONNECTICUT

DRAWN BXA 5/9/67
CHECKED
APPROVED
MATERIAL
FINISH
HEAT TREAT
PATTERN NO.

NAME: 700-1200 INTERFACE LOGIC
MODEL NO. GHA-1
DWG NO. C-23902
REV. B
SCALE
SHEET 2 OF 2